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EXAMINER	
NASH, LASHANYA RENEE	
ART UNIT	**PAPER NUMBER**
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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/941,619	COMEAU ET AL.	
	Examiner	Art Unit	
	LaShanya R. Nash	2153	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 August 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-86* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-86* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-86 are being considered.

Claim Objections

Claims 2-7 are objected to because of the following informalities: inconsistent terminology, and grammatical errors. Appropriate correction is required.

Examiner suggests replacing "The resource sharing system" recited in line 1 of claims 2-6 with "The system", so as to maintain consistent terminology with subsequent dependent claims.

Examiner suggests replacing "second processor core", recited in line 6 of claim 7 with "second processor", so as to maintain consistent terminology.

Examiner suggest replacing "A system", recited in line 1 of claims 30-31 with "The system", so as to maintain consistent terminology with subsequent dependent claims.

Examiner suggests replacing "first processing means" recited in line 2 of claim 80 with "a first processing means", so as to maintain consistent terminology.

Examiner suggests inserting "and" after semi-colon in line 4 of claim 84.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 60-75 is rejected under 35 U.S.C. 102(b) as being anticipated by Chennubhotla et al. (US Patent 5,841,988), hereinafter referred to as Chennubhotla.

In reference to claim 60, Chennubhotla discloses an interprocessor communication interface to facilitate the expedient and efficient exchange of information between processing elements in a multiprocessing environment, (abstract; column 1, lines 42 to column 2, line 6). Chennubhotla explicitly discloses:

- An interprocessor interface (Figures 1&2-item 2; columns 2-3) for interfacing between a first processor core (i.e. processing subsystem; Figure 1-item 12-1; columns 4-5) and a second processor core (i.e. processing subsystem; Figure 1-item 12-2), the interprocessor interface comprising:
- At least one data FIFO queue (i.e. receive FIFO buffer; Figure 2-item 126) having an input adapted to receive data from the second processor core and an output adapted to send data to the first processor core;
- At least one data FIFO queue (i.e. transmit FIFO buffer; Figure 2-item 124) having an input adapted to receive data from the first processor core and an output adapted to send data to the second processor core;
- A first out-of-band message transfer channel (i.e. interprocessor communications bus; Figures 1&2-item 18) for sending a message from the first processor core to the second processor core;
- A second out-of-band message transfer channel (i.e. local bus; Figure 2-item 108) for sending a message from the second processor core to the first processor core, (columns 4-6).

In reference to claim 61, Chennubhotla shows on a chip comprising an interprocessor interface in combination with the second processor core, (columns 1-5).

In reference to claim 62, Chennubhotla shows an interprocessor interface according to further comprising: a first interrupt channel adapted to allow the first processor core to interrupt the second processor core; and a second interrupt channel adapted to allow the second processor core to interrupt the first processor core, (columns 6-10; Figure 2-item 128).

In reference to claim 63, Chennubhotla shows an interprocessor interface according further comprising at least one register adapted to store an interrupt vector, (Figure 2-item 122; columns 6-10).

In reference to claim 64, Chennubhotla shows an interprocessor interface having functionality accessible by the first processor core memory mapped to a first memory space understood by the first processor core, and having functionality accessible by the second processor core memory mapped to a second memory space understood by the second processor core, (columns 5-6; Figure 2-item 20)

In reference to claim 65, Chennubhotla shows an interprocessor interface comprising a first access port comprising: a data port, an address port and a plurality of control ports, (columns 5-6; Figure 2-item 20)

In reference to claim 66, Chennubhotla shows an interprocessor interface wherein the control ports one or more of a group comprising chip select, write, read, interrupt, and DMA (direct memory access) interrupts, (columns 5-6; Figure 2-item 20).

In reference to claim 67, Chennubhotla shows an interprocessor interface further comprising chip select decode circuitry adapted to allow a chip select normally reserved for another chip to be used for the interprocessor interface over a range of addresses memory mapped to the interprocessor interface the range of addresses comprising at least a sub-set of addresses previously mapped to said another chip, (columns 6-9).

In reference to claim 68, Chennubhotla shows an interprocessor interface comprising a second access port comprising: a data port, an address port, and a control port, (columns 5-6; Figure 2-item 20).

In reference to claim 69, Chennubhotla shows an interprocessor interface in combination with the second processor, wherein the second access port is internal to the system on a chip, (columns 5-6; Figure 2-item 20).

In reference to claim 70, Chennubhotla shows an interprocessor interface further comprising at least one general-purpose input/output pin, (columns 5-10; Figure 2-item 122).

In reference to claim 71, Chennubhotla shows an interprocessor interface further comprising: a first plurality of memory mapped registers accessible to the first processor core, and a second plurality of memory mapped registers accessible to the second processor core, (columns 5-10; Figure 2-item 20).

In reference to claim 72, Chennubhotla shows an interprocessor interface wherein the second processor core has a sleep state in which the second processor core has a reduced power consumption, and in which the interprocessor interface remains active, (columns 7-12).

In reference to claim 73, Chennubhotla shows an interprocessor interface further comprising a register indicating the sleep state of the second processor core, (columns 5-7; Figure 2).

In reference to claim 74, Chennubhotla shows an interprocessor interface wherein the second processor core has a sleep mode in which the second processor core has a reduced power consumption, and in which the interprocessor interface remains active, (columns 7-12).

In reference to claim 75, Chennubhotla shows an interprocessor interface further comprising a register indicating the sleep state of the second processor core, (columns 7-12).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-7,11-20, 27-29,50-59, and 80-82 rejected under 35 U.S.C. 103(a) as being unpatentable over Chennubhotla above, and further in view of Dutta (US Patent Application Publication 2001/0047383), hereinafter referred to as Chennubhotla and Dutta.

In reference to claim 1, Chennubhotla discloses a system for interprocessor communication, in order to facilitate the expedient and efficient exchange of information between processing elements in a multiprocessing environment, (abstract; column 1, lines 42 to column 2, line 6). Chennubhotla explicitly discloses:

- A resource sharing system (i.e. multiprocessing system sharing system memory; Figures 1& 2;columns 2-3) comprising:
- A first processor (Figure 1-item 12-1) and a second processor (Figure 1-item 12-2), the first processor managing a resource (i.e. system memory; Figures 1&2-item 14) which is to be made available to the second processor (i.e. each processing subsystem processes instruction code out of system memory; column 4);
- A physical layer interconnection between the first processor and the second processor (i.e. interprocessor communications bus; Figures 1&2-item 18) a first application layer entity (i.e. data processing function/DSP Engine; Figure 2-items 102&103; column 1; column 5, lines 16-32) on the first processor and a corresponding second application layer entity on the second processor (i.e. DSP Engine; Figure 2-items 102&103), the first application layer entity and the second application layer entity together being adapted to arbitrate access (i.e. via the Memory controller/DMA; Figure 2-item 104) to the resource between the first processor and the second processor using the interprocessor communications protocol, (i.e. interprocessor communications protocol; columns 1-3; column 7), the physical layer interconnection and the intercommunications protocol to provide a communication channel between the first application

layer entity and the second application layer entity, (i.e. interprocessor communications interface and protocol used to pass data between processing elements; columns 4-6).

However, Chennubhotla fails to disclose the system comprises: a communications protocol comprising a first interprocessor communications protocol running on the first processor, and a second interprocessor communications protocol running on the second processor which is a peer to the first interprocessor communications protocol; and arbitrating access to the resource between the first processor and the second processor using the first interprocessor communications protocol, and the second intercommunications protocol to provide a communication channel between the first application layer entity and the second application layer entity. However, it would have been obvious to accordingly modify the aforementioned system, as disclosed by Chennubhotla, for one of ordinary skill in the art at the time of the invention, as further evidenced by Dutta.

In an analogous art, Dutta discloses a system for interprocessor communications between a processor and legacy devices operating under distinct protocols, (abstract). Dutta further discloses that the system comprises: a communications protocol (i.e. translation protocol; paragraphs [0030]-[0033]), comprising a first interprocessor communications protocol (i.e. common communications protocol; paragraph [0028]) running on the first processor (i.e. client computer; Figure 3-item 21; Figure 6), and a second interprocessor communications protocol (i.e. proprietary protocols; paragraph [0029]) running on the second processor (i.e. legacy device; Figure 2-item 17; Figure 3-item 47; Figure 8) which is a peer to the first interprocessor communications protocol; and arbitrating access using the first interprocessor communications protocol, and the second intercommunications protocol to provide a communication channel between the first application layer entity (i.e. application programs; paragraphs [0050]-[0054]; Figure 6-item 124) and the second application layer entity (i.e. legacy programs; paragraphs [0062]-[0066]; Figure 8-item 224), (paragraphs [0023]-[0033]). Thusly, one of ordinary skill in the art would have been motivated to accordingly modify the aforementioned system as disclosed by Chennubhotla, so as to support communicate interprocessor communication with legacy devices and thereby increasing system compatibility with various legacy devices available in the distributed environment, (Dutta; paragraphs [0003]-[0007]).

In reference to claim 80, Chennubhotla discloses a system for interprocessor communication, in order to facilitate the expedient and efficient exchange of information between processing elements in a multiprocessing environment, (abstract; column 1, lines 42 to column 2, line 6). Chennubhotla explicitly discloses:

- A resource sharing system (i.e. multiprocessing system sharing system memory; Figures 1& 2;columns 2-3) comprising:
- A first processing means (i.e. processing subsystem; Figure 1-item 12-1) and a second processing means (i.e. processing subsystem; Figure 1-item 12-2), the first processing means managing a resource (i.e. system memory; Figures 1&2-item 14) which is to be made available to the second processing means (i.e. each processing subsystem processes instruction code out of system memory; column 4);
- An interprocessor communications protocol means (i.e. interprocessor communications interface and protocol; Figure 1-item 20; columns 2-3);
- A physical layer interconnection means between the first processing means and the second processing means (i.e. interprocessor communications bus; Figures 1&2-item 18) a first application layer means (i.e. data processing function/DSP Engine; Figure 2-items 102&103; column 1; column 5, lines 16-32) on the first processing means and a corresponding second application layer means on the second processing means (i.e. DSP Engine; Figure 2-items 102&103), the first application layer means and the second application layer means together being adapted to arbitrate access (i.e. via the Memory controller/DMA; Figure 2-item 104) to the resource means between the first processing means and the second processing means using the interprocessor communications protocol means, (i.e. interprocessor communications protocol; columns 1-3; column 7), the physical layer interconnection means and the intercommunications protocol means to provide a communication channel between the first application layer means and the second application layer means, (i.e. interprocessor

communications interface and protocol used to pass data between processing elements; columns 4-6).

However, Chennubhotla fails to disclose the system comprises: a first interprocessor communications protocol means running on the first processing means, and a second interprocessor communications protocol means running on the second processing means which is a peer to the first interprocessor communications protocol means; and arbitrating access to the resource between the first processing means and the second processing means using the first interprocessor communications protocol means, and the second intercommunications protocol means to provide a communication channel between the first application layer means and the second application layer means. However, it would have been obvious to accordingly modify the aforementioned system, as disclosed by Chennubhotla, for one of ordinary skill in the art at the time of the invention, as further evidenced by Dutta.

In an analogous art, Dutta discloses a system for interprocessor communications between a processor and legacy devices operating under distinct protocols, (abstract). Dutta further discloses that the system comprises: a communications protocol means (i.e. protocol translator; paragraphs [0030]-[0033]), comprising a first interprocessor communications protocol means (i.e. common communications protocol; paragraph [0028]) running on the first processing means (i.e. client computer; Figure 3-item 21; Figure 6), and a second interprocessor communications protocol means (i.e. proprietary protocols; paragraph [0029]) running on the second processing means (i.e. legacy device; Figure 2-item 17; Figure 3-item 47; Figure 8) which is a peer to the first interprocessor communications protocol means; and arbitrating access using the first interprocessor communications protocol means, and the second intercommunications protocol means to provide a communication channel between the first application layer means (i.e. application programs; paragraphs [0050]-[0054]; Figure 6-item 124) and the second application layer means (i.e. legacy programs; paragraphs [0062]-[0066]; Figure 8-item 224), (paragraphs [0023]-[0033]). Thusly, one of ordinary skill in the art would have been motivated to accordingly modify the aforementioned system as disclosed by Chennubhotla, so as to support communicate interprocessor communication with legacy devices and thereby increasing system compatibility with various legacy devices available in the distributed environment, (Dutta; paragraphs [0003]-[0007]).

In reference to claim 2, Dutta shows the resource sharing system wherein arbitrating access to the resource between the first processor and the second processor comprises arbitrating access to the resource between one or more applications running on the first processor (i.e. application programs; Figure 6-item 124) and one or more applications (i.e. legacy programs; Figure 8-item 224) running on the second processor core, (paragraphs [0050]-[0067]).

In reference to claim 3, Chennubhotla shows the resource sharing system wherein the first application layer entity is a resource manager, (i.e. memory controller/DMA) and the second application layer entity is a peer resource manager (i.e. memory controller/DMA), (Figure 2-item 104; column 5, lines 11-36).

In reference to claims 4 and 81, Dutta shows the system further comprising an application layer state machine (i.e. program) running on at least one of the first and second processors adapted to define a state (i.e. status information) of the resource, (paragraph [0065]).

In reference to claim 5, Chennubhotla shows the system further comprising an interprocessor resource arbitration messaging protocol, (i.e. interprocessor communications interface and protocol; columns 2-3).

In reference to claims 6 and 82, Dutta shows the system further comprising: for each of a plurality of resources (i.e. legacy devices; Figure 2-items 17A-17C) to be shared, a respective first application layer entity on the first processor (i.e. application programs; Figure 6-item 124) and a respective corresponding second application layer entity on the second processor (i.e. legacy programs; paragraphs [0062]-[0066]; Figure 8-item 224), the respective first application layer entity and the respective second application layer entity together being adapted to arbitrate access to the resource between the first processor and the second processor, using the first interprocessor communications

protocol (i.e. common communications protocol; paragraph [0028]), the physical layer interconnection and the second intercommunications protocol (i.e. respective protocols X.Y,Z; paragraph [0029]) to provide a communication channel between the respective first application layer entity and the respective second application layer entity, (paragraphs [0023]-[0033]).

In reference to claim 7, Dutta shows the resource sharing system wherein arbitrating access to each resource (i.e. legacy devices; Figure 2-items 17A-17C) between the first processor and the second processor comprises arbitrating access to the resource between one or more applications running on the first processor (i.e. application programs; Figure 6-item 124) and one or more applications (i.e. legacy programs; Figure 8-item 224) running on the second processor core, (paragraphs [0050]-[0067]).

In reference to claim 11, Dutta shows the resource sharing system further comprising for each resource to be shared a respective resource specific interprocessor resource arbitration messaging protocol, (i.e. distinct protocols X, Y, Z; paragraph [0029]).

In reference to claim 12, Dutta shows the resource sharing system further comprising for each resource a respective application layer state machine (i.e. legacy programs; Figure 8-item 224) running on at least one of the first and second processors adapted to define a state (i.e. status information) of the resource.

In reference to claim 13, Dutta shows the system wherein: the first interprocessor communications protocol and the second interprocessor communications protocol are adapted to provide a respective resource-specific communications channel in respect of each resource, each resource-specific communications channel providing an interconnection between the application layer entities arbitrating use of the resource, (i.e. translation program provides a device –specific proprietary interface to the interface object/legacy device; Figure 3; paragraphs [0030]-[0033]).

In reference to claim 14, Dutta shows the system wherein: the first interprocessor communications protocol and the second interprocessor communications protocol are adapted to provide a respective resource-specific communications channel in respect of each resource; wherein at least one resource-specific communications channel provides an interconnection between the application layer entities arbitrating use of the resource; wherein at least one resource-specific communications channel maps directly to a processing algorithm called by the communications protocol, (i.e. translation program provides a device –specific proprietary interface to the interface object/legacy device; Figure 3; paragraphs [0030]-[0033]).

In reference to claim 15, Chennubhotla shows the system wherein for each resource-specific communications channel, the first interprocessor communications protocol and the second interprocessor communications protocol each have a respective receive queue and a respective transmit queue, (i.e. each interprocessor communications interface each has a respective Receive FIFO buffer and Transmit FIFO Buffer; Figure 1-items 20-1 to 20-n; Figure 2-item 124&126; columns 4-6).

In reference to claim 16, Chennubhotla shows the system wherein the first and second interprocessor communications protocols are adapted to exchange messages using a plurality of priorities, (i.e. pre-determined arbitration algorithms; column 5, line 41 to column 6, line 55).

In reference to claim 17, Chennubhotla shows the system wherein the first and second interprocessor communications protocols are adapted to exchange data using a plurality of priorities by providing a respective transmit channel queue and a respective receive channel queue for each priority, and by serving higher priority channel queues before lower priority queues, (i.e. pre-determined arbitration algorithms; columns 6-9).

In reference to claim 18, Dutta shows the system wherein at least one of the application layer entities is adapted to advise at least one respective third application layer entity of changes in the state of their respective resources, (paragraphs [0062]-[0066]).

In reference to claim 19, Dutta shows the system wherein each at least one respective third application layer entity is an application which have registered (i.e. paragraphs [0034]-[0037]) with one of the application layer entities to be advised of changes in the state of one or more particular resources, (paragraphs [0062]-[0067]).

In reference to claim 20, Dutta shows the system wherein each state machine (i.e. legacy program; Figure 8-item 224) maintains a state of the resource and identifies how incoming and outgoing messages of the associated resource specific messaging protocol affect the state of the state machine, (paragraphs [0028]-[0033]; paragraphs [0062]-[0067]).

In reference to claim 27, Dutta shows the system wherein a state machine is maintained on both processors for each resource, (paragraphs [0050]-[0066]; Figures 6&8).

In reference to claim 28, Dutta shows the system wherein the second interprocessor communications protocol further comprises a system observable having a system state machine and state controller, (paragraphs [0050]-[0066]; Figures 6&8).

In reference to claim 29, Dutta shows the system wherein messages in respect of all resources are routed through the system observable, thereby allowing conglomerate resource requests, (i.e. operate under one proprietary protocol; paragraph [0033]; paragraphs [0050]-[0066]; Figures 6&8).

In reference to claim 49, Chennubhotla shows the system wherein the physical layer interconnection is a serial link, (Figure 1-item 18).

In reference to claim 50, Chennubhotla shows the system wherein the physical layer interconnection is an HPI (host processor interface), (Figure 1-item 20).

In reference to claim 51, Chennubhotla shows the system wherein the physical layer interconnection is a shared memory arrangement, (Figure 1-item 14; column 5).

In reference to claim 52, Chennubhotla shows the system wherein the physical layer interconnection comprises an in-band messaging channel and an out-of-band messaging channel.

In reference to claim 53, Chennubhotla shows the system wherein the out-of-band messaging channel comprises at least one hardware mailbox, (column 5; column 5).

In reference to claim 54, Chennubhotla shows the system wherein the at least one hardware mailbox comprises at least one mailbox for each direction of communication, (column 5; Figure 2).

In reference to claim 55, Chennubhotla shows the system wherein the in-band messaging channel comprises a hardware FIFO, (Figure 2-items 124&126).

In reference to claim 56, Chennubhotla shows the system wherein the in-band messaging channel comprises a pair of unidirectional hardware FIFOs, (Figure 2-items 124&126).

In reference to claim 57, Chennubhotla shows the system wherein the in-band messaging channel comprises a shared memory location, (Figure 2-item 14).

In reference to claim 58, Chennubhotla shows the system wherein the out-of-band messaging channel comprises a hardware mailbox, the hardware mailbox causing an interrupt on the appropriate processor, (columns 5-6).

In reference to claim 59, Chennubhotla shows the system wherein an out-of-band message to a particular processor causes an interrupt on the processor to receive the out-of-band message and causes activation of an interrupt service routine which is adapted to parse the message, (columns 5-6).

In reference to claim 76, Chennubhotla shows the system wherein the physical layer interconnection between the first processor and the second processor comprises an interprocessor interface (Figures 1&2-item 2; columns 2-3) for interfacing between a first processor core (i.e. processing subsystem; Figure 1-item 12-1; columns 4-5) and a second processor core (i.e. processing subsystem; Figure 1-item 12-2), the interprocessor interface comprising: at least one data FIFO queue (i.e. receive FIFO buffer; Figure 2-item 126) having an input adapted to receive data from the second processor core and an output adapted to send data to the first processor core; at least one data FIFO queue (i.e. transmit FIFO buffer; Figure 2-item 124) having an input adapted to receive data from the first processor core and an output adapted to send data to the second processor core; a first out-of-band message transfer channel (i.e. interprocessor communications bus; Figures 1&2-item 18) for sending a message from the first processor core to the second processor core; a second out-of-band message transfer channel (i.e. local bus; Figure 2-item 108) for sending a message from the second processor core to the first processor core, (columns 4-6).

In reference to claim 77, Chennubhotla shows the system wherein the interprocessor interface further comprising: a first interrupt channel adapted to allow the first processor core to interrupt the second processor core; and a second interrupt channel adapted to allow the second processor core to interrupt the first processor core, (columns 6-10; Figure 2-item 128).

In reference to claim 78, Chennubhotla shows the system wherein the interprocessor interface further comprising at least one register adapted to store an interrupt vector, (Figure 2-item 122; columns 6-10).

In reference to claim 79, Chennubhotla shows the system wherein the interprocessor interface having functionality accessible by the first processor core memory mapped to a first memory space understood by the first processor core, and having functionality accessible by the second processor core memory mapped to a second memory space understood by the second processor core, (columns 5-6; Figure 2-item 20).

Claims 8-10, 21-26, 30-48, and 83-86 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chennubhotla and Dutta, as applied to claims 1 and 80, and further in vie w of Walter C. Dietrich, Jr. (Saving a Legacy with Objects [ACM]), hereinafter referred to as Dietrich.

In reference to claims 8 and 83, the Chennubhotla shows the system wherein the interprocessor communications protocol is designed to leave undisturbed real-time profiles of existing real-time functions of the processor running the other of the two interprocessor communications protocols, (columns 6-10). However the references, Chennubhotla and Dutta, fail to expressly show the system wherein one of the two interprocessor communications protocols is designed for efficiency and orthogonality between application layer entities running on the processor running the one of the two interprocessor communications protocols. Nonetheless, this was a well-known feature in the art at the time of invention, as further evidenced by Dietrich. Therefore, it would have been obvious to accordingly modify the system as disclosed by Chennubhotla and Dutta, for one of ordinary skill in the art at the time of invention.

In an analogous art, Dietrich discloses a legacy-based object-oriented interface to a legacy system, *(Introduction*, page 77). Dietrich further discloses that the system is designed for efficiency and orthogonality between application layer entities running on the processor, (*Increased Orthogonality*, page 81). One of ordinary skill in the art would have been so motivated to accordingly modify the system so as to increase system efficiency, (Dietrich; *Increased Orthogonality*, page 81).

In reference to claim 9, Chennubhotla shows the system wherein the first processor is a host processor, and the second processor is a coprocessor adding further functionality to the host processor, (column 1, lines 42-57; column 4, lines 44-65).

In reference to claim 10, Dutta shows the resource sharing system wherein the host processor has a message passing mechanism (i.e. operating system; paragraphs [0050]-[0054]; Figure 6-items 120) outside of the first interprocessor communications protocol to communicate between the first interprocessor communications protocol and the first application layer entity.

In reference to claim 21, Chennubhotla shows the system wherein the second interprocessor communications protocol comprises a channel thread domain which provides at least two different priorities over the physical layer interconnection, (i.e. bus arbiter; Figure 1-item 22; columns 8-9).

In reference to claim 22, Chennubhotla shows the system wherein the channel thread domain runs as part of a physical layer ISR (interrupt service routine), (columns 8-10).

In reference to claim 23, Chennubhotla shows the system wherein the channel thread domain provides at least two different priorities and a control priority, (i.e. pre-determined arbitration algorithms; columns 6-9).

In reference to claim 24, Dutta shows the system wherein for each resource, the respective second application layer entity comprises an incoming message listener, an outgoing message producer and a state controller, (paragraphs [0062]-[0066]; Figure 8).

In reference to claim 25, Dutta shows the system wherein the state controller and outgoing message producer are on one thread specific to each resource, and the incoming message listener is a separate thread that is adapted to serve a plurality of resources, (paragraphs [0062]-[0066]; Figure 8).

In reference to claim 26, Dutta shows the system wherein for each resource, the second application layer entity is entirely event driven and controlled by an incoming message listener, (paragraphs [0062]-[0066]; Figure 8).

In reference to claim 30, Dutta shows the system wherein each second application layer entity has a common API (application interface), (paragraphs [0062]-[0066]; Figure 8).

In reference to claim 31, Dutta shows the system wherein the common API comprises, for a given application layer entity, one or more interfaces in the following group: an interface for an application to register with the application layer entity to receive event notifications generated by this application layer entity; an interface for an application to de-register from the application layer entity to no longer receive event notifications generated by this application layer entity; an interface for an application to temporarily suspend the notifications from the application layer entity; an interface for an application to end the suspension of the notifications from that application layer entity; an interface to send data to the corresponding application layer entity; and an interface to invoke a callback function from the application layer entity to another application, (paragraphs [0034]-[0066]).

In reference to claim 32, Chennubhotla shows the system further comprising: for each resource a respective receive session queue and a respective transmit session queue in at least one of the first interprocessor communications protocol and the second interprocessor communications protocol, (i.e. respective transmit FIFO and Receive FIFO for each interprocessor communications interface; columns 5-9; Figures 1&2).

In reference to claim 33, Chennubhotla shows the system further comprising: for each of a plurality of different priorities, a respective receive channel queue and a respective transmit channel queue in at least one of the first interprocessor communications protocol and the second interprocessor communications protocol, (i.e. respective transmit FIFO and Receive FIFO for each interprocessor communications interface; columns 5-9; Figures 1&2).

In reference to claim 34, Chennubhotla shows the system further comprising on at least one of the two processors, a physical layer service routine adapted to service the transmit channel queues by dequeueing channel data elements from the transmit channel queues starting with a highest priority transmit channel queue and transmitting the channel data elements thus dequeued over the physical layer interconnection, and to service the receive channel queues by dequeueing channel data elements from the physical layer interconnection and enqueueing them on a receive channel queue having a priority matching that of the dequeued channel data element, (columns 6-10; Figure 2-items 124,122,126).

In reference to claim 35, Chennubhotla shows the system wherein on one of the two processors, the transmit channel queues and receive channel queues are serviced on a scheduled basis, the system further comprising on the one of the two processors, a transmit buffer between the transmit channel queues and the physical layer interconnection and a receive buffer between the receive physical layer interconnection and the receive channel queues, wherein the output of the transmit channel queues is copied to the transmit buffer which is then periodically serviced by copying to the physical layer interconnection, and wherein received data from the physical layer interconnection is emptied into the receive buffer which is then serviced when the channel controller is scheduled, (columns 6-10; Figure 2-items 124,122,126).

In reference to claim 36, Chennubhotla shows the system wherein each transmit session queue is bound to one of the transmit channel queues, each receive session queue is bound to one of the receive channel queues and each session queue is given a priority matching the channel queue to which the session queue is bound, the system further comprising: a session thread domain adapted to dequeue from the transmit session queues working from highest priority session queue to lowest priority session queue and to enqueue on the transmit channel queue to which the transmit session queue is bound, and to dequeue from the receive channel queues working from the highest priority channel

queue to the lowest priority channel queue and to enqueue on an appropriate receive session queue, the appropriate receive session queue being determined by matching an identifier in that which is to be enqueued to a corresponding session queue identifier, (columns 6-10; Figure 2-items 124,122,126).

In reference to claim 37, Chennubhotla shows the system wherein data/messages is transmitted between corresponding application layer entities managing a given resource in frames; wherein the session thread domain converts each frame into one or more packets; wherein the channel thread domain converts each packet into one or more blocks for transmission, (columns 5-7).

In reference to claim 38, Chennubhotla shows the system wherein blocks received by the channel controller are stored a data structure comprising one or more blocks, and a reference to the data structure is queued for the session layer thread domain to process, (columns 5-8).

In reference to claim 39, Chennubhotla shows the system further comprising, for each of a plurality of [queue, peer queue] pairs implemented by the first and second interprocessor communications protocols, a respective flow control protocol, (columns 6-9).

In reference to claim 40, Chennubhotla shows the system further comprising: for each of a plurality of [transmit session queue, peer receive session queue] pairs implemented by the first and second interprocessor communications protocols, a respective flow control protocol, wherein the session thread is adapted to handle congestion in a session queue; for each of a plurality of [transmit channel queue, peer receive channel queue] pairs implemented by the first and second interprocessor communications protocols, a respective flow control protocol, wherein the channel controller handles congestion on a channel queue, (columns 6-12).

In reference to claim 41, Chennubhotla shows the system wherein the session controller handles congestion in a receive session queue with flow control messaging exchanged through an in-band control channel, (columns 5-9).

In reference to claim 42, Chennubhotla shows the system wherein the physical layer ISR handles congestion in a receive channel queue with flow control messaging exchanged through an out-of-band channel, (columns 5-9).

In reference to claim 43, Chennubhotla shows the system wherein congestion in a transmit session queue is handled by the corresponding application entity, (columns 5-9).

In reference to claim 44, Chennubhotla shows the system wherein congestion in a transmit channel queue is handled by the session thread by holding any channel data element directed to the congested queues and letting traffic queue up in the session Queues, (columns 5-10).

In reference to claim 45, Chennubhotla shows the system wherein the interprocessor communications protocol designed to mitigate the effects on the real-time profile further comprises an additional buffer between the physical layer interconnection a scheduled combined channel controller/session manager function adapted to perform buffering during periods between scheduling of the combined channel controller/session manager, (columns 5-10).

In reference to claim 46, Chennubhotla shows the system wherein the first interprocessor communications protocol interfaces with application layer entities using a message-passing mechanism provided by the processor the external to the first interprocessor communications protocol of the first processor, each application layer entity being a resource manager, (columns 5-10).

In reference to claim 47, Chennubhotla shows the system wherein the first interprocessor communications protocol is implemented with a single thread acting as a combined channel controller and session manager, (columns 5-10).

In reference to claim 48, Chennubhotla shows the system wherein the first interprocessor communications protocol is implemented with a single system task acting as a combined channel controller and session manager, (columns 5-10).

In reference to claim 84, Dutta shows the resource sharing system further comprising for each resource to be shared a respective resource specific interprocessor resource arbitration messaging protocol, (i.e. distinct protocols X, Y, Z; paragraph [0029]); and for each resource a respective application layer state machine (i.e. legacy programs; Figure 8-item 224) running on at least one of the first and second processors adapted to define a state (i.e. status information) of the resource.

In reference to claim 85, Chennubhotla shows the system wherein the first and second interprocessor communications protocols are adapted to exchange data using a plurality of priorities by providing a respective transmit channel queue and a respective receive channel queue for each priority, and by serving higher priority channel queues before lower priority queues, (i.e. pre-determined arbitration algorithms; columns 6-9).

In reference to claim 86, Dutta shows the system wherein each state machine (i.e. legacy program; Figure 8-item 224) maintains a state of the resource and identifies how incoming and outgoing messages of the associated resource specific messaging protocol affect the state of the state machine, (paragraphs [0028]-[0033]; paragraphs [0062]-[0067]).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to LaShanya R Nash whose telephone number is (571) 272-3957. The examiner can normally be reached on 9am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Glenton Burgess can be reached on (571) 272-3949. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

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